Remarks/Arguments

Claim 18 appeared twice in the priority application. This discrepency was corrected by preliminary amendment dated March 12, 2002 canceling claim 18. Claims 5, 18, 19, 22, 30 and 31 are canceled by the present amendment. New claims 32 and 33 are ~~is~~ added by the present amendment. The underlined portions of these remarks highlight corrections to this amendment made by the applicant pursuant to the examiner's telephone request of July 13, 2004. The applicant hereby re-submits this corrected amendment to the Office via facsimile for further consideration by the examiner.

35 U.S.C. §103¶

Claims 1,2,4-9,11-17,20-24, 26-31 stand rejected under 35 U.S.C. 103(x) as being unpatentable over Tsuji et al. U.S. Pat. No. 5,111,297.

The office action states independent claim 1 is a method claim of independent claim 14. Claim 1 is rejected for the same reasons as claim 14. Further, the office action states independent claim 9 is a method claim of claim 14 and rejected claim 9 for the same reasons as claim 14. Independent claim 23 was rejected for the same reasons as claim 14. Therefore, for ease of discussion, applicant will discuss rejection of independent claims 1, 9 and 14 and 23 together in the following paragraphs.

Claim 1 is amended herein to recite:

"A method for multiplying the frame rate of an input video signal comprising the steps of:

simultaneously providing said input video signal to a delay memory and a speed-up memory to provide a delayed video signal and a speeded up video signal;

speeding up said delayed video signal to provide a delayed speeded up input video signal;

alternately supplying at least a portion of said speeded up video signal and at least a portion of said delayed speeded up video signal to a liquid crystal display.

Claim 14 is amended herein to recite:

A frame rate multiplier for an input video signal comprising:

a delay memory and a first speed up memory for receiving said input video signal;

a second speed up memory coupled to an output of said delay memory for speeding up said delayed video signal;

a multiplexer coupled to said first and second speed up memories;

a display coupled to said multiplexer such that **portions of video supplied by said multiplexer to said display originate alternately from said first and second speed up memories.**

Claim 9 is amended herein to recite:

"A method for multiplying the frame rate of a video signal comprising the steps of:

delaying said input video signal for a time less than one frame period;

speeding up said delayed video signal;

speeding up said input video signal;

alternately supplying lines of said speeded up video signal and lines of said delayed speeded up video signal; and,

writing said alternately supplied lines into a liquid crystal display.

Claim 23 has been amended to recite:

"A frame rate doubler comprising:

a first memory for delaying said input video signal;

a second memory for speeding up said delayed video signal;

a third memory for speeding up said input video signal;

a multiplexer coupled to said second and third memories so as to **alternately select video signals output from said second and third memories** for writing to a liquid crystal display."

With regard to claims 1, 9, 14 and 23, the office action states Tsuji (Second Frame Memory 22, Fig. 6) discloses a first memory for said input video signal, said first memory having a maximum required data storage capacity just large enough to delay said input video signal for a fraction of a frame period 1/fvin. Please note applicant has removed language limiting the claim 1, 9, 14 and 23 embodiments of the invention to any particular storage capacity so as not to unduly limit the scope of the invention. Further, applicant has amended claim 14 to more clearly recite the following novel structure in a frame rate multiplier. That is, **one of applicant's memories for receiving an input signal comprises**

a time delay memory while another memory receiving the same input signal comprises a speed up memory. Support for applicant's amended claim language can be found in applicant's specification, for example, on page 9, lines 12 - 15.

None of the cited prior art, including Tsuji, discloses a multiplier structure wherein an input video signal is provided to two memories, each memory having different timing functions (a time delay memory and a speed up memory). Tsuji, for example, discloses that second frame memory 22 and first frame memory 21 of Tsuji Fig. 6 serve the same function with respect to the portion of the input signal they contain.

For explanation see Tsuji col. 5 lines 56-59, "The figure [6] is intended to for better understanding of the operation of FIG. 4, and actually the operational control is implemented through the control of the reading reset pulses for the first and second memories 5 and 6 [of Fig 4]."

Memories 5 and 6 of Figure 4 of Tsuji are disclosed as memories for storing a single frame of sub picture video. (Tsuji is directed to a PIP apparatus). Tsuji teaches that memories 5 and 6 store one frame of video each. See, for example Tsuji, col. 5 lines 12-19, "The one-frame memories 5 and 6 store video signals for two fields, i.e., the contents of field A and field B respectively of the sub-picture video signal." Fuji fails to disclose time delaying the signal in one memory and speeding it up in the other (claim 14), simultaneously providing the input video signal to a delay memory and a speed-up memory (claim 1) and delaying said input video signal for a time less than one frame period (claim 9).

Further, Tsuji fails to disclose a display coupled to a multiplexer such that portions of video supplied by the multiplexer to the display originate alternately from first and second speed up memories, wherein one of the speed up memories provides a delayed speeded up video signal and the other provides a speeded up video signal (claim 14). Likewise, Tsuji fails to disclose simultaneously providing said input video signal to a delay memory and a speed-up up memory to provide a delayed video signal and a speeded up video signal and speeding up the delayed video signal to provide a delayed speeded up input video signal, followed by a step of alternately supplying at least a portion of the speeded up video signal and at least a portion of the delayed speeded up video signal to a liquid crystal display (claim 1).

This limitation in applicant's claim is supported by applicant's specification, for example, on page 9 lines 16-21, " The delayed video signal is speeded up by a 2:1 speedup memory 18. The output signal 20 of speedup memory 18 is both delayed and speeded up."

Applicant's delay memory need not store a whole frame, i.e., in one embodiment, the delay memory comprises a partial frame memory (see applicant's claim 15).

Furthermore, Tsuji fails to disclose or suggest a frame memory storing less than one frame of video, nor does Tsuji disclose a frame rate multiplier capable of operating with a frame memory storing less than one frame as claimed in applicant's dependent claims 2 and 15.

Regarding claim 15, the office action states Tsuji does not specify how large the memories are. The office action states it would have been obvious matter of design choice to modify the Tsuji reference by having a first memory that is'/ of a frame or 2/3, 3/4 or, 4/5 of a frame, etc. The office action asserts applicant has not disclosed that having such size difference would solve any stated problem or is for any particular purpose. The office action states "it appears that any other memory would perform equally well."

Applicant respectfully disagrees. First, Tsuji does specify how large the memories are. Tsuji specifically discloses memories 5 and 6 as "one frame memories" that store one frame of video each. In that regard, applicant respectfully directs the attention of the office to Tsuji, col. 5 lines 12-19 : "The one-frame memories 5 and 6 store video signals for two fields, i.e., the contents of field A and field B respectively of the sub-picture video signal."

Second, applicant has both disclosed and clearly stated that size difference (embodiments of applicant's invention having a memory storing less than one frame) solves a problem of prior art memories, including the memory of Tsuji. (Please see applicant's specification page 5 lines 8-23):

> "In accordance with the prior art, frame rate doublers utilize two full frame memories in a so-called ping-pong arrangement. A frame is written into one memory as another frame is read out of the other memory, and vice versa, in an alternating manner. This technique always incurs a full frame period of video delay because neither of the ping-pong frame memories can be read out until a full frame has been written in. Accordingly, the audio signal must be delayed to match the video delay. It was known that the memory requirements could be reduced to one full frame memory by proper utilization of the memory in a correctly implemented video speedup arrangement. However, for any frame multiplication greater than doubling, the alternative use of one full frame memory is not workable. Two full frame memories are always required in such a situation."

Further, applicant's specification describes a particular purpose for applicant's memory storing less than one frame. (see page 6 lines 13-24):

> " In the case of a frame rate doubler, for example, this advantageously allows a one-half frame memory to be used instead of a full frame memory, and advantageously reduces the memory bandwidth required. The memory size reduction is very important, because a half-frame memory can be embedded on an integrated circuit providing other functions, whereas a full frame memory is too large, or at least, too expensive to embed. Moreover, it is advantageously not necessary to delay the audio to match the frame rate multiplied video, as in the ping-pong memory arrangement. "

The remaining claims in applicant's specification depend from claims 1, 9 14 and 23. Having fully addressed the Examiner's rejections with regard to the independent claims, it is believed this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at (609) 734-6892, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,

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